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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,717	11/14/2003	Anthony David Williams	030772	2063
26285	5285 7590 04/13/2005		EXAMINER	
KIRKPATRICK & LOCKHART NICHOLSON GRAHAM LLP 535 SMITHFIELD STREET PITTSBURGH, PA 15222			NGUYEN, LINH M	
			ART UNIT	PAPER NUMBER
	•		2816	
			DATE MAILED: 04/13/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)					
· · · · · · · · · · · · · · · · · · ·	10/713,717	WILLIAMS, ANTHONY DAVID					
Office Action Summary	Examiner	Art Unit					
	Linh M. Nguyen	2816					
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address					
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply if NO period for reply is specified above, the maximum statutory period we Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	66(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days ill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONEI	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).					
Status							
1) Responsive to communication(s) filed on 14 No.	ovember 2003.						
2a) ☐ This action is FINAL . 2b) ☑ This	☐ This action is FINAL . 2b)☑ This action is non-final.						
• • • • • • • • • • • • • • • • • • • •	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 45	53 O.G. 213.					
Disposition of Claims							
4) Claim(s) 1-19 is/are pending in the application.	☑ Claim(s) <u>1-19</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdraw	4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.	Claim(s) is/are allowed.						
6) Claim(s) <u>1-5 and 16-19</u> is/are rejected.							
7) Claim(s) 6-15 is/are objected to.							
8) Claim(s) are subject to restriction and/or	election requirement.						
Application Papers							
9) The specification is objected to by the Examine	r.						
10)⊠ The drawing(s) filed on 14 November 2003 is/ar	10)⊠ The drawing(s) filed on <u>14 November 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the o	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.					
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the prior application from the International Bureau * See the attached detailed Office action for a list of	s have been received. s have been received in Application ity documents have been received (PCT Rule 17.2(a)).	on No ed in this National Stage					
Amash	•						
Attachment(s) 1) ☑ Notice of References Cited (PTO-892)	4) Interview Summary	(PTO-413)					
2) D Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da	ate					
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/14/03.	5) Notice of Informal P 6) Other:	atent Application (PTO-152)					

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DETAILED ACTION

Claims 1-19 are presented in the instant application according to the Applicant's filing on 11/14/2003.

Specification Objection

1. The specification is objected to because of the following minor informalities:

Page 8, paragraph [0022], line 1, change "31" to --30--;

line 5, change "10" to --32--;

line 6, change "31" to --30--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 5, 16-17 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Meltzer et al. (U.S. Pub. No. 2004/0223575).

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With respect to claim 1, Meltzer et al. discloses, in Fig. 1, a frequency synthesizer, comprising a phase locked loop including an analog mixer phase detector [13] (see US Pub. No. 2003/0058961, Fling et al., paragraph [0129], line 1, for the term "PLL mixer/phase detector"), and an auxiliary digital frequency detector [15] coupled to the phase locked loop.

With respect to claim 2, Meltzer et al. further discloses, in Fig. 1, a programmable divider [23] having an input terminal responsive to an output signal of the frequency synthesizer and having an output terminal coupled to an input terminal of the analog mixer phase detector [13]; a loop filter [27] having an input terminal coupled to an output terminal of the analog mixer phase detector; and a voltage controlled oscillator [11] having a control terminal coupled to an output terminal of the loop filter.

With respect to claim 3, Meltzer et al. discloses, in Fig. 1, that the analog mixer phase detector [13] is for detecting a phase difference between the output signal of the programmable divider and a reference signal [from 21].

With respect to claim 5, Meltzer et al. discloses, in Fig. 1, that the auxiliary digital frequency detector [15] has a first input terminal coupled to the output terminal of the programmable divider [23].

With respect to claim 16, Meltzer et al. discloses, in Fig. 1, a frequency synthesizer, comprising a phase locked loop including an analog mixer phase detector [13] (see US Pub. No. 2003/0058961, Fling et al., paragraph [0129], line 1, for the term "PLL mixer/phase detector"); and means [15] for making the analog mixer phase detector automatically acquire phase lock when the phase locked loop is out of lock.

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With respect to claim 17, Meltzer et al. further discloses, in Fig. 1, a programmable divider [23] having an input terminal responsive to an output signal of the frequency synthesizer and having an output terminal coupled to an input terminal of the analog mixer phase detector [13]; a loop filter [27] having an input terminal coupled to an output terminal of the analog mixer phase detector; and a voltage controlled oscillator [11] having a control terminal coupled to an output terminal of the loop filter.

With respect to claim 19, Meltzer et al. discloses, in Fig. 1, a frequency synthesizer including a voltage controlled oscillator [11], a loop filter [27], and an analog mixer phase detector [13] (see US Pub. No. 2003/0058961, Fling et al., paragraph [0129], line 1, for the term "PLL mixer/phase detector"), a method comprising adjusting the voltage applied to the voltage controlled oscillator from the loop filter until the frequency of an output signal of the analog mixer phase detector is within a pass-band of the loop filter.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meltzer et al. (U.S. Pub. No. 2004/0223575) in view of Hartman et al. (U.S. Patent No. 6,359,476).

With respect to claims 4 and 18, Meltzer et al. discloses all of the claimed limitations as expressly recited in claims 1-2 and 16-17, respectively. However, Meltzer et al. does not explicitly disclose the programmable divider being a direct digital synthesizer or including a

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direct digital synthesizer; Hartman et al. discloses in column 6, line 27-28, that a direct digital synthesizer is essentially a digital frequency divider for providing an incremental resolution. To include a direct digital synthesizer in the programmable divider or to employ a direct digital synthesizer as a programmable divider within the frequency synthesizer of Meltzer et al. for providing frequency accuracy (see col. 5, line 51) would have been obvious to one of ordinary skills in the art at the time of the invention since including a direct digital synthesizer in the programmable divider or employing a direct digital synthesizer as a programmable divider has been well-known in the art as evident by the teachings of Hartman et al.

Allowable Subject Matter

- 5. Claims 6-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 6. The following is a statement of reasons for the indication of allowable subject matter:

 The closest prior art of record does not show or fairly suggest:
- a) A frequency synthesizer including a comparator being coupled between the output terminal of the programmable divider and the first input terminal of the auxiliary digital frequency detector, as called for in claim 6; and
- b) A frequency synthesizer including a differential integrator circuit having an input terminal responsive to an output signal of the auxiliary digital frequency detector, and in which an output terminal of the differential integrator circuit is coupled to the loop filter, as called for in claim 7.

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Citation of Relevant Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Riley (U.S. Patent No. 6,404,291) discloses a linear low noise phase loop frequency synthesizer using controlled divider pulse widths.

Prior art Bogdan (U.S. Patent No. 5,910,753) discloses direct digital phase synthesis.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN DIMARY EXAMINER